

BEST AVAILABLE COPY

Appl. No. 10/605,193
Amdt. dated February 27, 2006
Reply to Office action of November 28, 2005

REMARKS/ARGUMENTS

Claims 1, 8, and 15 have been amended to better point out distinct differences of the current invention. Claims 6 and 14 have been cancelled, and claim 5 has been slightly amended to take care of informalities. No new material has been introduced. Reconsideration of claims 1-5, 7-13, and 15-20 is respectfully requested.

Claims 1-5, 8-13, and 15-20 have been rejected under 34 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Wolaver (U.S. 4,590,502). Claims 6, 7, and 14 are objected to as being dependant upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Applicant has chosen to amend claim 1 to include limitations found in allowed claim 6 and claim 6 has been cancelled. No new material has been introduced.

The added limitation states "before adjusting the frequency of the clock according to the updated estimate rate in the dithering step, if a phase difference or frequency difference between the clock and the input signal exceeds a predetermined value, the frequency of the clock is adjusted according to the updated estimated rate in the dithering step". As alluded to by the Examiner, these limitations in combination with claim 1 are not taught in known prior art and are believed to be allowable.

Similarly, claim 8 has been amended to include limitations found in allowed claim 14 and claim 14 has been cancelled. No new material has been introduced. Again, as alluded to by the Examiner, these limitations in combination with claim 8 are not taught in known prior art and are believed to be allowable.

Furthermore, independent claim 15, previously comprising the limitation of "setting a dithering estimated value as a new comparing clock when a synchronization error between the comparing clock and the input signal exceeds a predetermined value", has been amended to include limitations of "setting the frequency adjustment value as the new comparing clock when the synchronization error between the comparing clock and

BEST AVAILABLE COPY

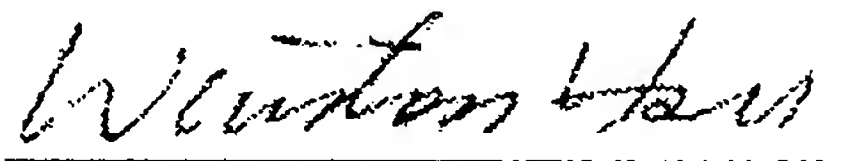
Appl. No. 10/605,193
Amdt. dated February 27, 2006
Reply to Office action of November 28, 2005

the input signal does not exceed the predetermined value". Cited prior art seems to indicate that the Examiner referred to as "dithered" signal is always used for comparisons, which is functionally different than using it only when the error exceeds a predetermined value and not using the "dithered" signal when the error does not exceed the predetermined value. This distinction is similar to limitations found in allowed claims 5 6 and 7 and no new material has been introduced. As such, the Applicant believes that claim 15 should now also be allowable.

Because the allowability of dependent claims ultimately depends upon the allowability of their respective base claims, it is believed that all claims in the application should now be allowable and respectfully requests reconsideration of claims 1-5, 7-13, 10 and 15-20 and requests that a timely Notice of Allowance be issued in this case should the Examiner concur.

Sincerely yours,

15



Date: 02.27.2006

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

20 Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

25